TC40H107P/F
TC40H107AP/AF

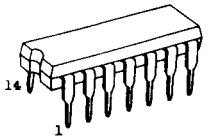
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H107 DUAL J-K FLIP-FLOP (PULSE TRIGGER TYPE)
TC40H107A DUAL J-K FLIP-FLOP (EDGE TRIGGER TYPE)

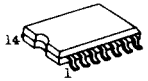
The TC40H107 is a dual J-K flip - flop with clear function.

For J-K mode, if $\overline{\text{CLEAR}}$ input is set to "H" level and clock is provided, the output Q and $\overline{Q}$ of the TC40H107 change at the clock 1 pulse and the TC40H107A at the falling edge of clock, according to the state of J and K.

When $\overline{\text{CLEAR}}$ input is set to "L" level, Q attains "L" level, and $\overline{Q}$ attains "H" level, regardless of other inputs.



DIP14(3D14A-P)

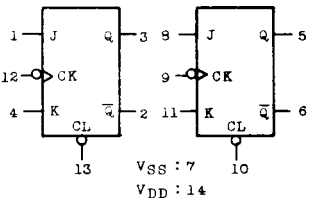


MFP14(F14GB-P)

MAXIMUM RATING

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C • 10 sec	

BLOCK DIAGRAM



* ALL INPUTS ARE EQUIPPED WITH PROTECTION CIRCUIT.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	-	8.0	V
Input Voltage	V_{IN}	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-40	-	85	°C

TRUTH TABLE (TC40H107)

INPUTS				OUTPUTS	
$\overline{\text{CLEAR}}$	$\overline{\text{CLOCK}}$	J	K	Q	$\overline{Q}$
L	*	*	*	L	H
H	⎍	L	L	NO CHANGE	
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

TRUTH TABLE (TC40H107A)

INPUTS				OUTPUTS	
$\overline{\text{CLEAR}}$	$\overline{\text{CLOCK}}$	J	K	Q	$\overline{Q}$
L	*	*	*	L	H
H	⎌	L	L	NO CHANGE	
H	⎌	H	L	H	L
H	⎌	L	H	L	H
H	⎌	H	H	TOGGLE	
H	⎍	*	*	NO CHANGE	

* = Don't Care
⎍ = One high-Level Pulse
⎍ = Transition from Low to high level.
⎌ = Transition from high to Low level.

ELECTRICAL CHARACTERISTIC (V_{SS}=0.0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	-	0.05	-	0.0	0.05		0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V V_{IN}=V_{SS},V_{DD}	5	1.4	-	1.1		-	0.8	-	
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-		1.0	-	1.0	
Input Current	"H" Level	I_{IH}	I_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	*V_{IN}=V_{SS},V_{DD}	5	-	5.0	-	10^{-2}	5.0	-	25.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTIC (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rist Time		t_{or}	CIRCUIT 1	-	18	40	ns
Output Fall Time		t_{of}		-	15	40	
Propagation Delay Time	(Low-High)	t_{pLH}	CIRCUIT 1 $\overline{CLOCK}$-Q,$\bar{Q}$	-	25	38	ns
	(High-Low)	t_{pHL}		-	35	52	
	(Low-High)	t_{pLH}	CIRCUIT 1 $\overline{CLEAR}$-Q,$\bar{Q}$	-	24	38	ns
	(High-Low)	t_{pHL}		-	35	52	
Min. Clear pulse width		t_w	CIRCUIT 1 $\overline{CLEAR}$	-	20	40	ns
Max. Clock Frequency		$f_{max\phi}$		10	20	-	MHz
Max. Clock Rise Time Max. Clock Fall Time		$t_{r\phi}$ $t_{f\phi}$		1.0	3.0	-	μs
Min. Data Setup Time		t_{set-up}	CIRCUIT 3 TC40H107A	-	-	35	ns
Min. Data Setup Time		t_{set-up}	CIRCUIT 2 TC40H107	-	-	0	ns
Min. Data Hold Time		t_{hold}	CIRCUIT 3 TC40H107A	-	-	15	ns
Min. Data Hold Time		t_{hold}	CIRCUIT 2 TC40H107	-	-	0	ns
Input Capacitance		C_{IN}		-	5		pF
Min. Clear Removal Time		t_{rem}	CIRCUIT 1 TC40H107A	-	28	40	ns
Min. Clear Removal Time		t_{rem}	CIRCUIT 1 TC40H107	-	18	35	ns

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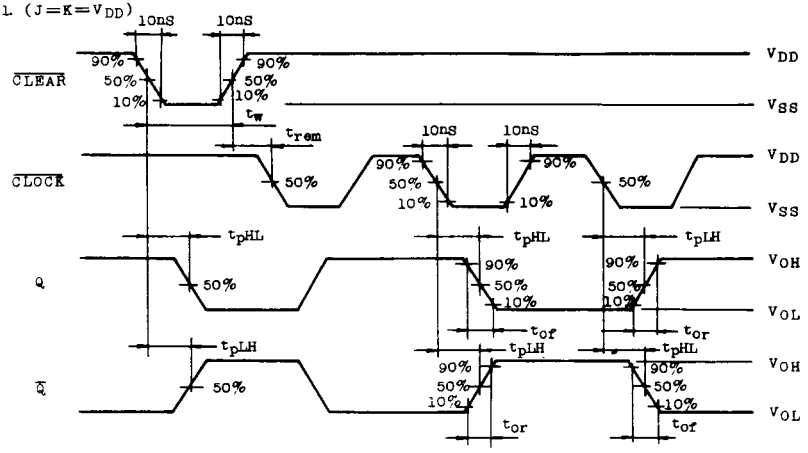
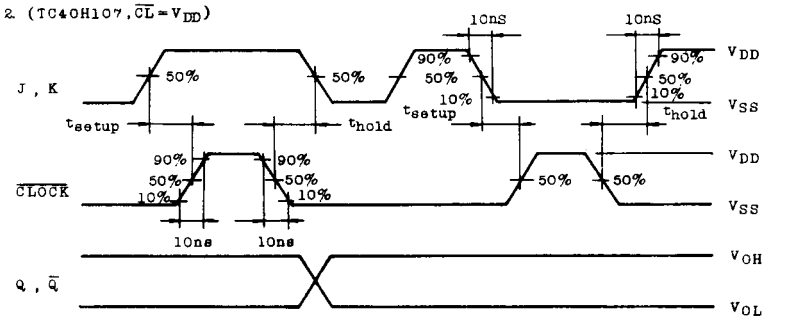
SWITCHING TIME TEST WAVEFORM

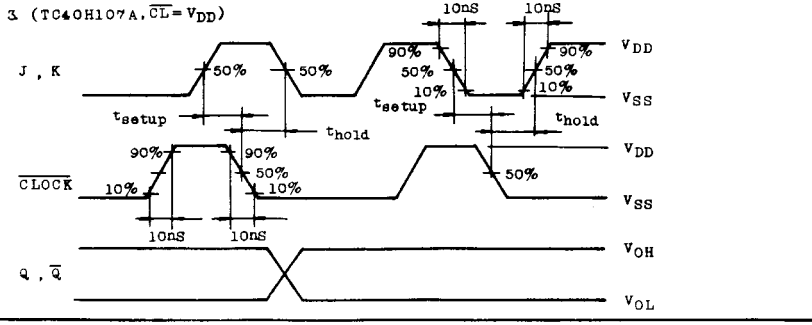
CIRCUIT 1. (J=K=V_{DD})



CIRCUIT 2. (TC40H107, $\overline{CL}$=V_{DD})



CIRCUIT 3. (TC40H107A, $\overline{CL}$=V_{DD})



TC40H107P/F
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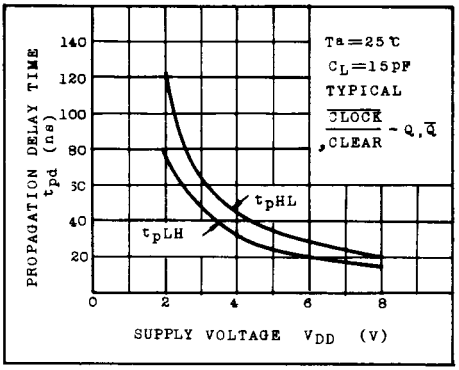
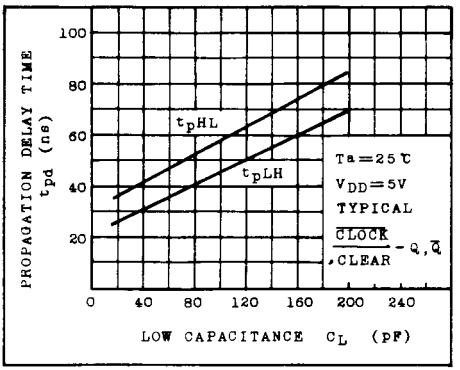
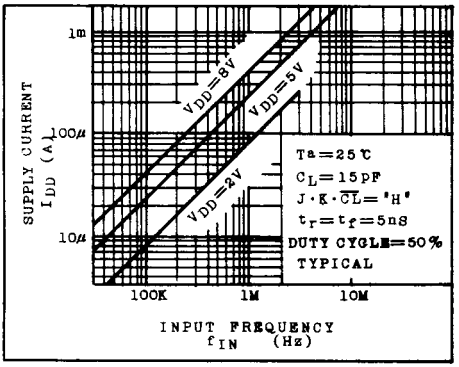
t_{pd} - V_{DD}



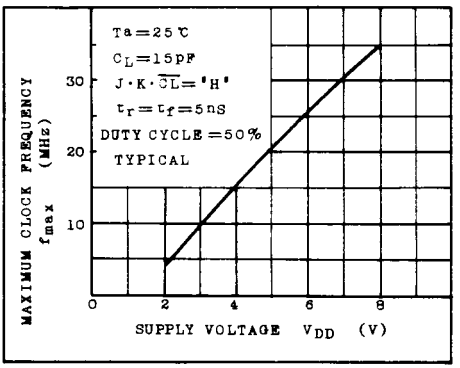
t_{pd} - C_L



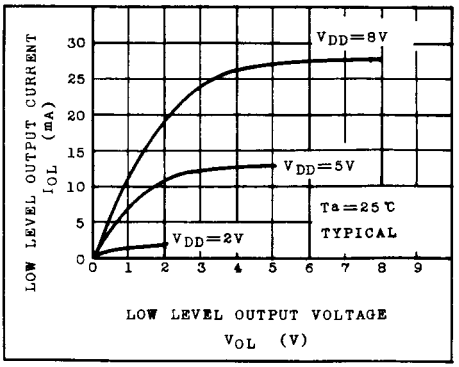
f_{IN} - I_{DD}/FF



f_{max} - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})