COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4089B

PRELIMINARY DATA

BINARY RATE MULTIPLIER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO "15" INPUT AND "15" DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS

The **HCC 4089B** (extended temperature range) and **HCF 4089B** (intermediate temperature range) are monolithic integrated circuit available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4089B** is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses.
The **HCC/HCF 4089B** has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in timing diagram.
If more than one binary input bit is high, the resulting pulse train is a combination of the above separate pulse trains. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

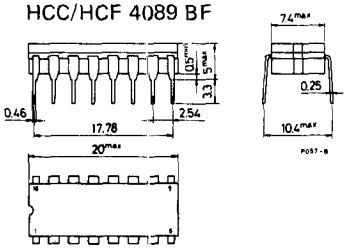
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

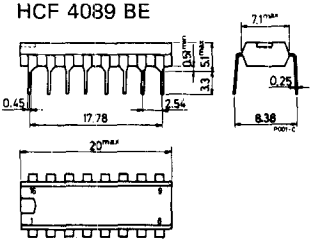
HCC 4089 BD	for dual in-line ceramic package
HCC 4089 BF	for dual in-line ceramic package, frit seal
HCC 4089 BK	for ceramic flat package
HCF 4089 BE	for dual in-line plastic package
HCF 4089 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

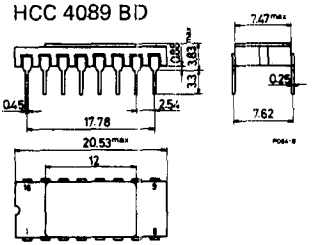
Dual in-line ceramic package for HCC/HCF 4089 BF



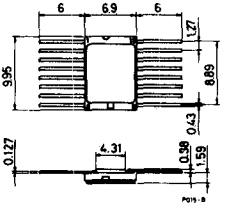
Dual in-line plastic package for HCF 4089 BE



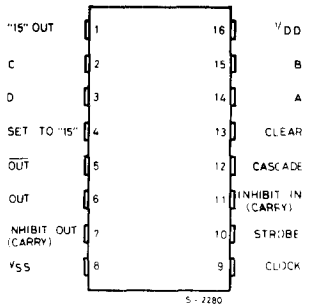
Dual in-line ceramic package for HCC 4089 BD



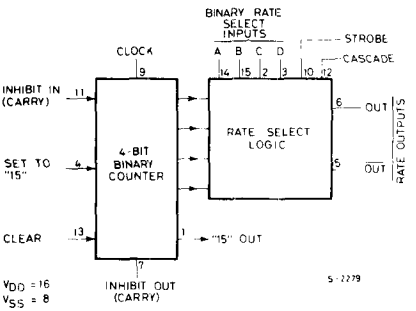
Ceramic flat package for HCC 4089 BK



CONNECTION DIAGRAM



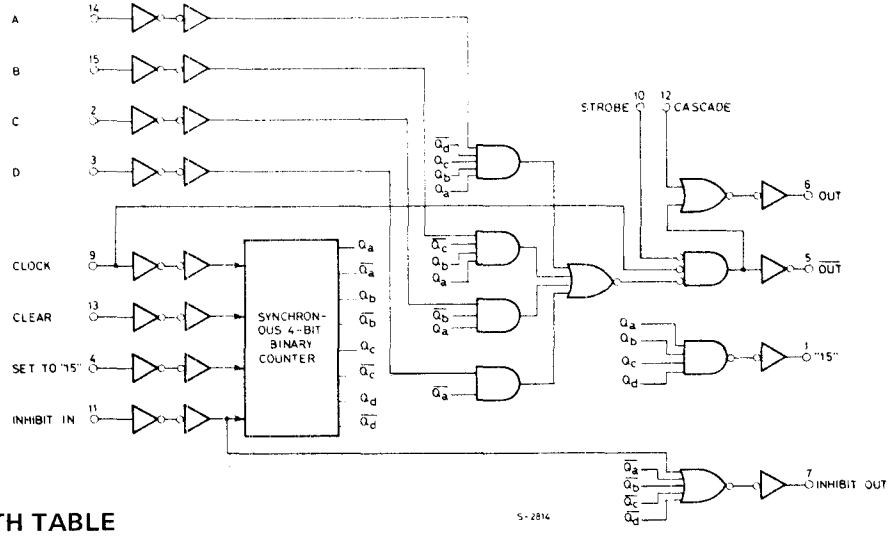
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for HCC types	-55 to 125	°C
	for HCF types	-40 to 85	°C

LOGIC DIAGRAM



TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	●	●	H	●
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).
● Depends on internal state of counter.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

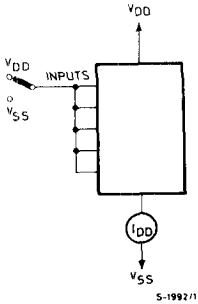
Parameter		Test conditions	V_{DD} (V)	Values Min.	Typ.	Max.	Unit
t_{PHL}, t_{PLH} Propagation delay time	Clock to out		5		110	220	ns
			10		55	110	
			15		45	90	
	Clock or strobe to out		5		150	300	ns
			10		75	150	
			15		60	120	
	Clock to inhibit high level to low level		5		360	720	ns
			10		160	320	
			15		110	220	
	Low level to high level		5		250	500	ns
			10		100	200	
			15		75	150	
	Clear to out		5		380	760	ns
			10		175	350	
			15		130	260	
	Clock to "9" or "15" out		5		300	600	ns
			10		125	250	
			15		90	180	
	Cascade to out		5		90	180	ns
			10		45	90	
			15		35	70	
	Inhibit in to inhibit out		5		160	320	ns
			10		75	150	
			15		55	110	
	Set to out		5		330	660	ns
			10		150	300	
			15		110	220	
t_{THL}, t_{TLH} Transition time			5		100	200	ns
			10		50	100	
			15		40	80	
f_{CL} Maximum clock frequency			5	1.2	2.4		MHz
			10	2.5	5		
			15	3.5	7		
t_W Clock pulse width			5	330	165		ns
			10	170	85		
			15	100	50		
t_r, t_f Clock rise or fall time			5			15	μs
			10			15	
			15			15	
t_W Set or clear pulse width			5	160	80		ns
			10	90	45		
			15	60	30		

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

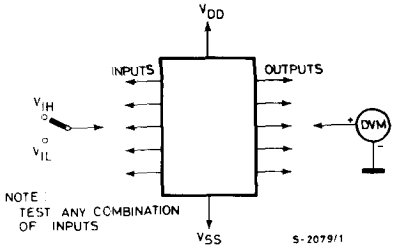
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{setup}	Inhibit input setup time, high level to low level	5	100	50		ns
		10	40	20		
		15	20	10		
t_R	Inhibit, input removal time	5	240	120		ns
		10	130	65		
		15	110	55		
t_R	Minimum set removal time	5	150	75		ns
		10	80	40		
		15	50	25		
t_R	Clear removal time	5	60	30		ns
		10	40	20		
		15	30	15		

TEST CIRCUIT

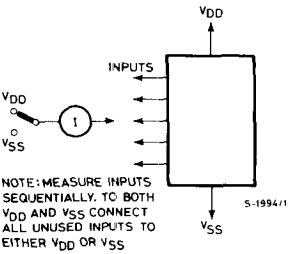
Quiescent device current



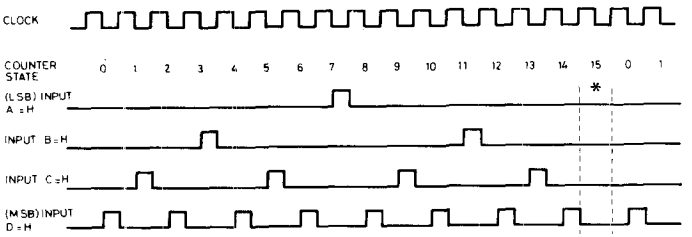
Noise immunity



Input leakage current



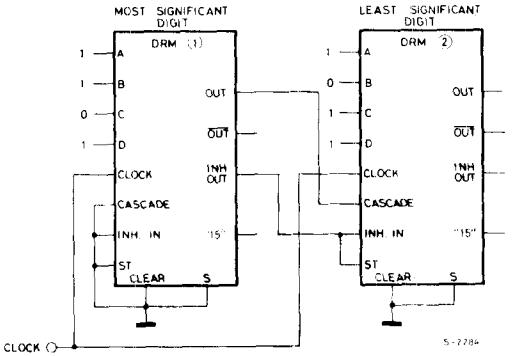
TIMING DIAGRAM



APPLICATION NOTES

For words of more than 4 bits, **HCC/HCF 4089B** devices may be cascaded in two different modes: an Add mode and a Multiply mode.

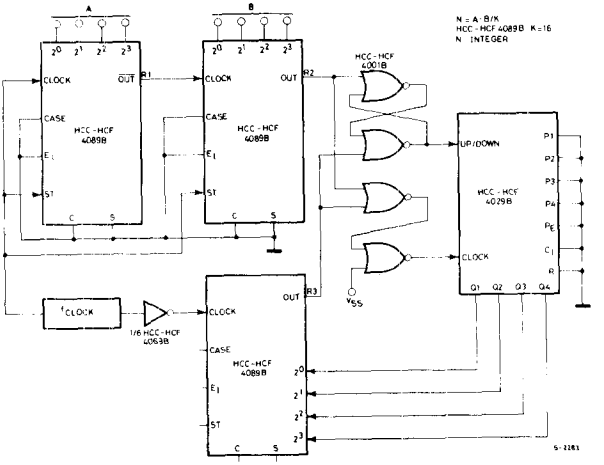
Two **HCC/HCF 4089B**'s cascaded in the "Add" mode with a preset number of 189.



Nota:
In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

Two **HCC/HCF 4089B**'s cascaded in the Multiply mode for Multiplication of two variables A and B with loop circuit control.



When the loop stabilises rate R_2 = rate R_3, thus $f_{clock}\ (\frac{A}{16} \cdot \frac{B}{16}) = f_{clock}\ (\frac{1}{16} \cdot \frac{N}{16})$ therefore $N = A \cdot B$.