

HEF4044B

Quad R/S latch with 3-state outputs

Rev. 10 — 18 November 2011

Product data sheet

1. General description

The HEF4044B is a quad R/S latch with 3-state outputs, with a common output enable input (OE). Each latch has an active LOW set input ($\overline{1S}$ to $\overline{4S}$), an active LOW reset input ($\overline{1R}$ to $\overline{4R}$) and an active HIGH 3-state output ($1Q$ to $4Q$).

When OE is HIGH, the latch output (nQ) is determined by the $n\overline{R}$ and $n\overline{S}$ inputs as shown in [Table 3](#). When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. The high impedance off-state feature allows common bussing of the outputs.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- Four-bit storage with output enable

4. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| HEF4044BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| HEF4044BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |



5. Functional diagram

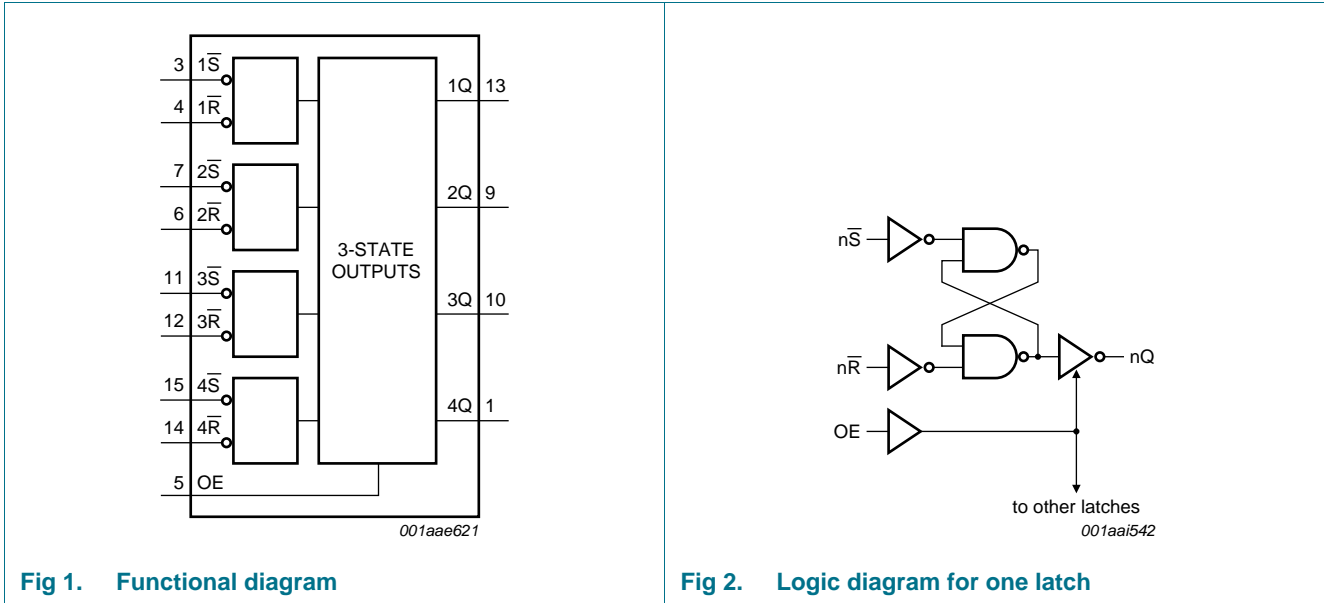


Fig 1. Functional diagram

Fig 2. Logic diagram for one latch

6. Pinning information

6.1 Pinning

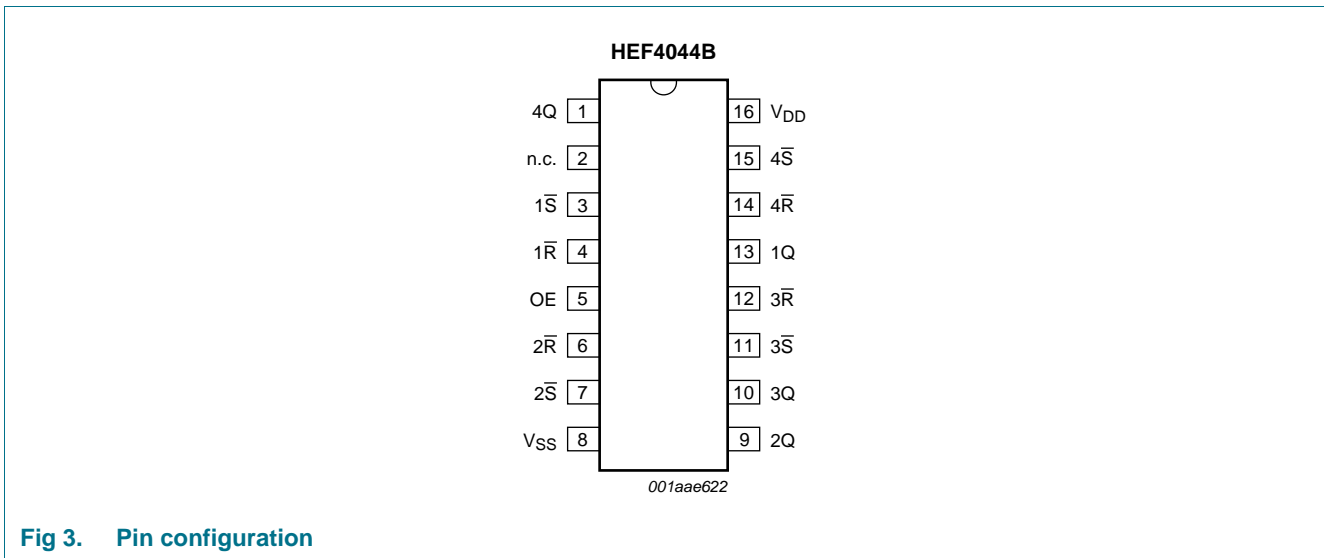


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------|--------------|-------------------------------|
| n.c. | 2 | not connected |
| $1\bar{S}$ to $4\bar{S}$ | 3, 7, 11, 15 | set input (active LOW) |
| $1\bar{R}$ to $4\bar{R}$ | 4, 6, 12, 14 | reset input (active LOW) |
| OE | 5 | common output enable input |
| V_{SS} | 8 | ground supply voltage |
| 1Q to 4Q | 13, 9, 10, 1 | 3-state buffered latch output |
| V_{DD} | 16 | supply voltage |

7. Functional description

Table 3. Function table^[1]

| Input | | | | Output |
|-------|------------|------------|---------|--------|
| OE | $n\bar{S}$ | $n\bar{R}$ | nQ | |
| L | X | X | Z | |
| H | L | H | H | |
| H | X | L | L | |
| H | H | H | latched | |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance state.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------|-------------------------|--|------|----------------|------|----|
| V_{DD} | supply voltage | | -0.5 | +18 | V | |
| I_{IK} | input clamping current | $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | - | ± 10 | mA | |
| V_I | input voltage | | -0.5 | $V_{DD} + 0.5$ | V | |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V | - | ± 10 | mA | |
| $I_{I/O}$ | input/output current | | - | ± 10 | mA | |
| I_{DD} | supply current | | - | 50 | mA | |
| T_{stg} | storage temperature | | -65 | +150 | °C | |
| T_{amb} | ambient temperature | | -40 | +85 | °C | |
| P_{tot} | total power dissipation | T_{amb} -40 °C to +85 °C | | | | |
| | | DIP16 package | [1] | - | 750 | mW |
| | | SO16 package | [2] | - | 500 | mW |
| | | per output | - | - | 100 | mW |

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|------------------------|-----|-----|----------|-----------------|
| V_{DD} | supply voltage | | 3 | - | 15 | V |
| V_I | input voltage | | 0 | - | V_{DD} | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD} = 5\text{ V}$ | - | - | 3.75 | $\mu\text{s/V}$ |
| | | $V_{DD} = 10\text{ V}$ | - | - | 0.5 | $\mu\text{s/V}$ |
| | | $V_{DD} = 15\text{ V}$ | - | - | 0.08 | $\mu\text{s/V}$ |

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{amb} = -40\text{ °C}$ | | $T_{amb} = 25\text{ °C}$ | | $T_{amb} = 85\text{ °C}$ | | Unit |
|----------|---------------------------|---|----------|---------------------------|-----------|--------------------------|-----------|--------------------------|-----------|---------------|
| | | | | Min | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| V_{IL} | LOW-level input voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| V_{OH} | HIGH-level output voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| V_{OL} | LOW-level output voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| I_{OH} | HIGH-level output current | $V_O = 2.5\text{ V}$ | 5 V | - | -1.7 | - | -1.4 | - | -1.1 | mA |
| | | $V_O = 4.6\text{ V}$ | 5 V | - | -0.52 | - | -0.44 | - | -0.36 | mA |
| | | $V_O = 9.5\text{ V}$ | 10 V | - | -1.3 | - | -1.1 | - | -0.9 | mA |
| | | $V_O = 13.5\text{ V}$ | 15 V | - | -3.6 | - | -3.0 | - | -2.4 | mA |
| I_{OL} | LOW-level output current | $V_O = 0.4\text{ V}$ | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O = 0.5\text{ V}$ | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O = 1.5\text{ V}$ | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| I_I | input leakage current | | 15 V | - | ± 0.3 | - | ± 0.3 | - | ± 1.0 | μA |
| I_{OZ} | OFF-state output current | nQ output HIGH; returned to V_{DD} | 15 V | - | 1.6 | - | 1.6 | - | 12.0 | μA |
| | | nQ output LOW; returned to V_{SS} | 15 V | - | 1.6 | - | 1.6 | - | 12.0 | μA |

Table 6. Static characteristics ...continued
 $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{amb} = -40\text{ }^{\circ}\text{C}$ | | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | | $T_{amb} = 85\text{ }^{\circ}\text{C}$ | | Unit |
|----------|-------------------|--------------------|----------|---|-----|--|-----|--|-----|---------------|
| | | | | Min | Max | Min | Max | Min | Max | |
| I_{DD} | supply current | $I_O = 0\text{ A}$ | 5 V | - | 20 | - | 20 | - | 150 | μA |
| | | | 10 V | - | 40 | - | 40 | - | 300 | μA |
| | | | 15 V | - | 80 | - | 80 | - | 600 | μA |
| C_I | input capacitance | | | - | - | - | 7.5 | - | - | pF |

11. Dynamic characteristics

Table 7. Dynamic characteristics
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see [Figure 6](#); unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | Extrapolation formula | Min | Typ | Max | Unit |
|-----------|-------------------------------------|--|----------|---|-----|-----|-----|------|
| t_{PHL} | HIGH to LOW propagation delay | \overline{nR} to nQ; see Figure 4 | 5 V | [1] $63\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 90 | 185 | ns |
| | | | 10 V | $29\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 40 | 80 | ns |
| | | | 15 V | $22\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 30 | 60 | ns |
| t_{PLH} | LOW to HIGH propagation delay | \overline{nS} to nQ; see Figure 4 | 5 V | [1] $63\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 90 | 180 | ns |
| | | | 10 V | $29\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 40 | 80 | ns |
| | | | 15 V | $22\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 30 | 60 | ns |
| t_t | transition time | see Figure 4 | 5 V | [1] $10\text{ ns} + (1.00\text{ ns/pF})C_L$ | - | 60 | 120 | ns |
| | | | 10 V | $9\text{ ns} + (0.42\text{ ns/pF})C_L$ | - | 30 | 60 | ns |
| | | | 15 V | $6\text{ ns} + (0.28\text{ ns/pF})C_L$ | - | 20 | 40 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | OE \rightarrow nQ; see Figure 5 | 5 V | | - | 50 | 100 | ns |
| | | | 10 V | | - | 30 | 60 | ns |
| | | | 15 V | | - | 25 | 50 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | OE \rightarrow nQ; see Figure 5 | 5 V | | - | 30 | 60 | ns |
| | | | 10 V | | - | 25 | 45 | ns |
| | | | 15 V | | - | 20 | 40 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | OE \rightarrow nQ; see Figure 5 | 5 V | | - | 50 | 100 | ns |
| | | | 10 V | | - | 25 | 50 | ns |
| | | | 15 V | | - | 20 | 40 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | OE \rightarrow nQ; see Figure 5 | 5 V | | - | 50 | 95 | ns |
| | | | 10 V | | - | 25 | 45 | ns |
| | | | 15 V | | - | 20 | 35 | ns |
| t_W | pulse width | \overline{nS} input LOW; minimum width; see Figure 4 | 5 V | | 30 | 15 | - | ns |
| | | | 10 V | | 20 | 10 | - | ns |
| | | | 15 V | | 16 | 8 | - | ns |
| | | \overline{nR} input LOW; minimum width; see Figure 4 | 5 V | | 30 | 15 | - | ns |
| | | | 10 V | | 20 | 10 | - | ns |
| | | | 15 V | | 16 | 8 | - | ns |

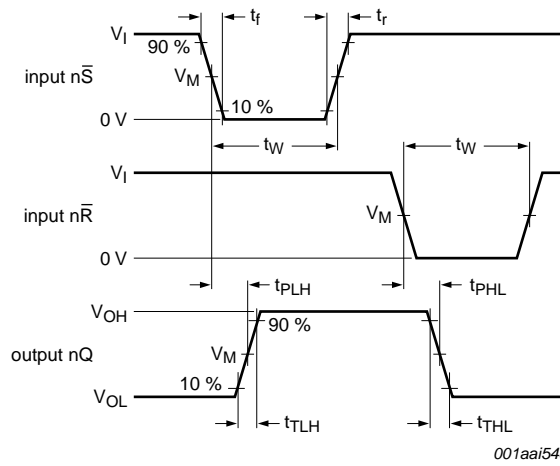
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

| Symbol | Parameter | V_{DD} | Typical formula for P_D (μW) | where: |
|--------|---------------------------|----------|---|---|
| P_D | dynamic power dissipation | 5 V | $P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f_i = input frequency in MHz, |
| | | 10 V | $P_D = 5200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f_o = output frequency in MHz, |
| | | 15 V | $P_D = 12900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs. |

12. Waveforms



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Set ($n\bar{S}$) and reset ($n\bar{R}$) inputs pulse width and propagation delay to latch output (nQ) and output nQ transition time

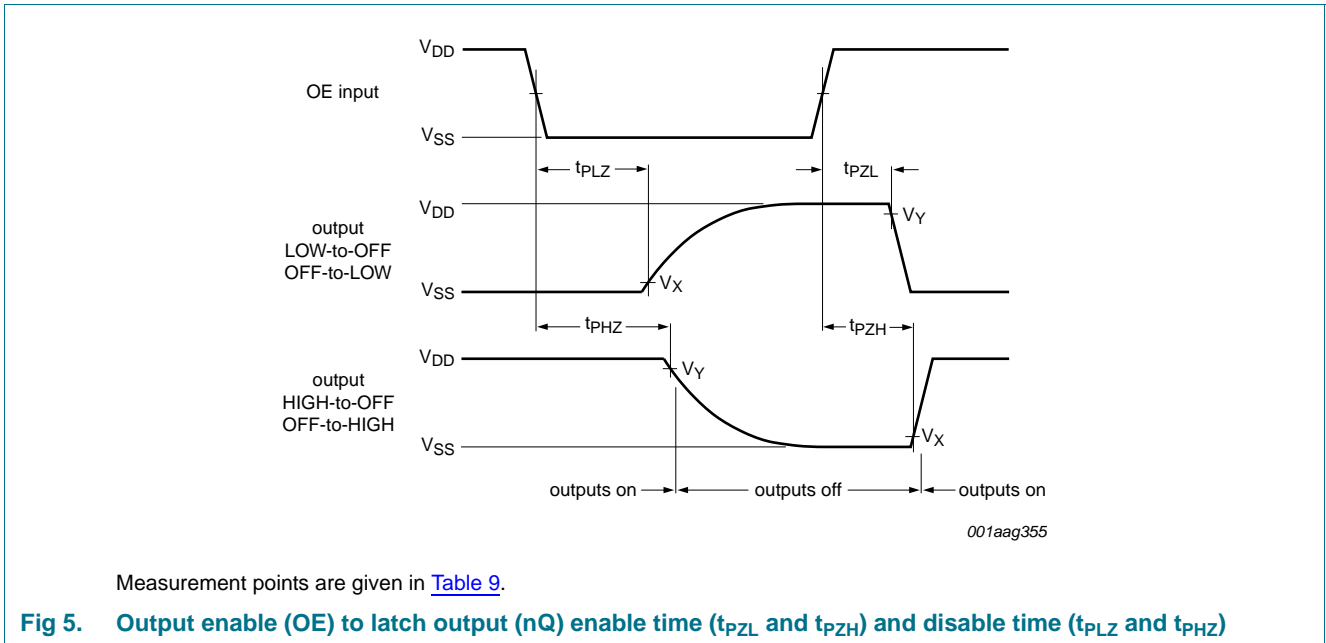
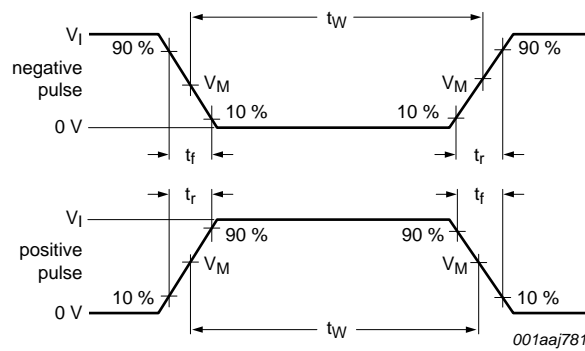
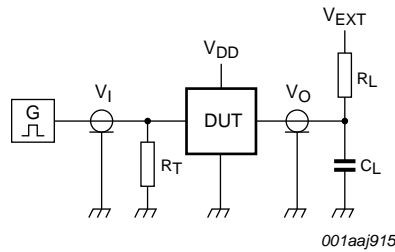


Table 9. Measurement points

| Supply voltage | Input | | Output | | |
|-----------------|------------------------------------|--------------------|--------------------|--------------------|--------------------|
| V _{DD} | V _I | V _M | V _M | V _X | V _Y |
| 5 V to 15 V | V _{DD} or V _{SS} | 0.5V _{DD} | 0.5V _{DD} | 0.1V _{DD} | 0.9V _{DD} |



a. Input waveform



b. Test circuit

Test and measurement data is given in [Table 10](#).

Definitions test circuit:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 6. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|----------------|----------|--------------|-------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PLZ}, t_{PZL} | t_{PHZ}, t_{PZH} |
| 5 V to 15 V | V_{DD} | ≤ 20 ns | 50 pF | 1 k Ω | open | V_{DD} | GND |

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

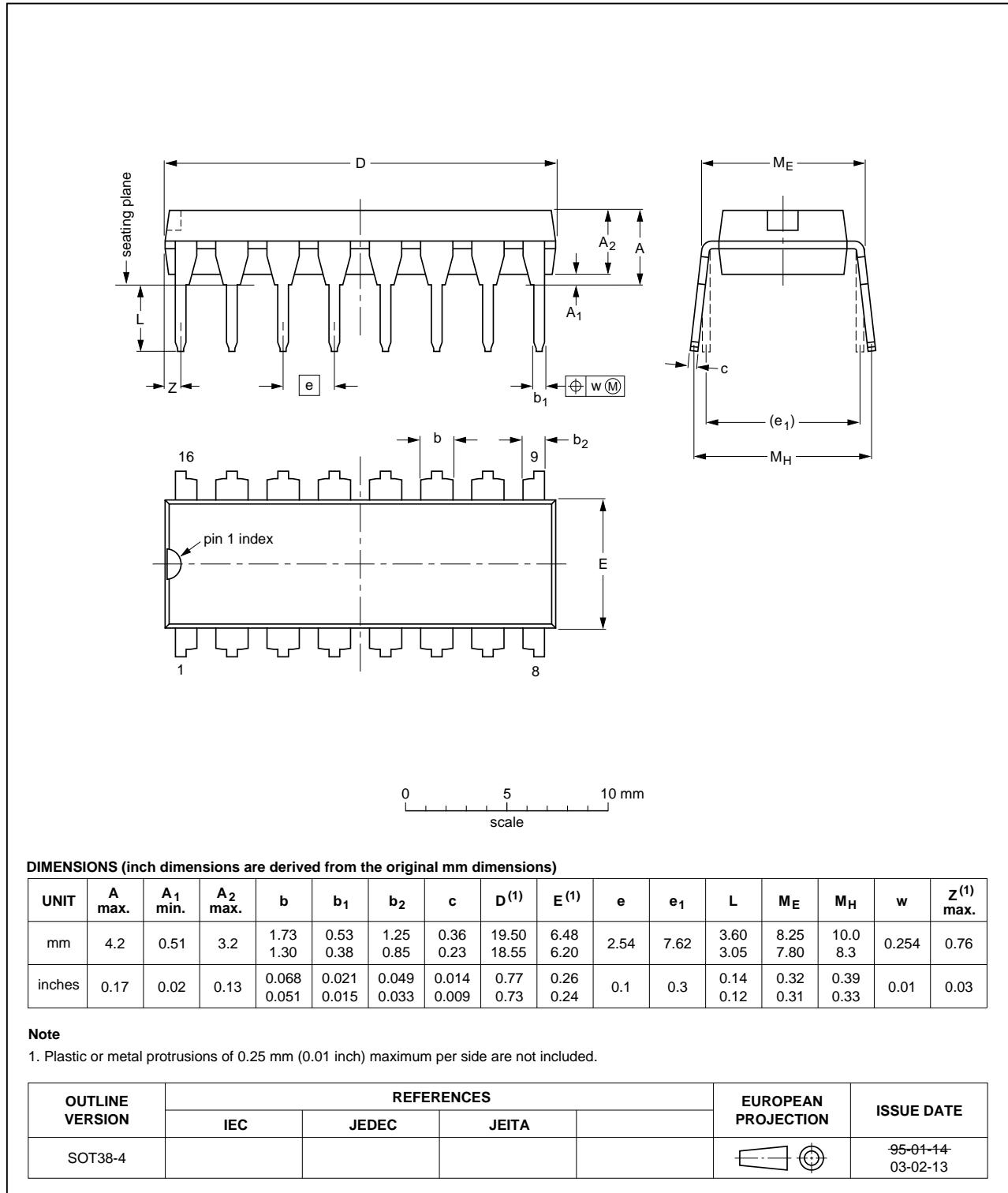


Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

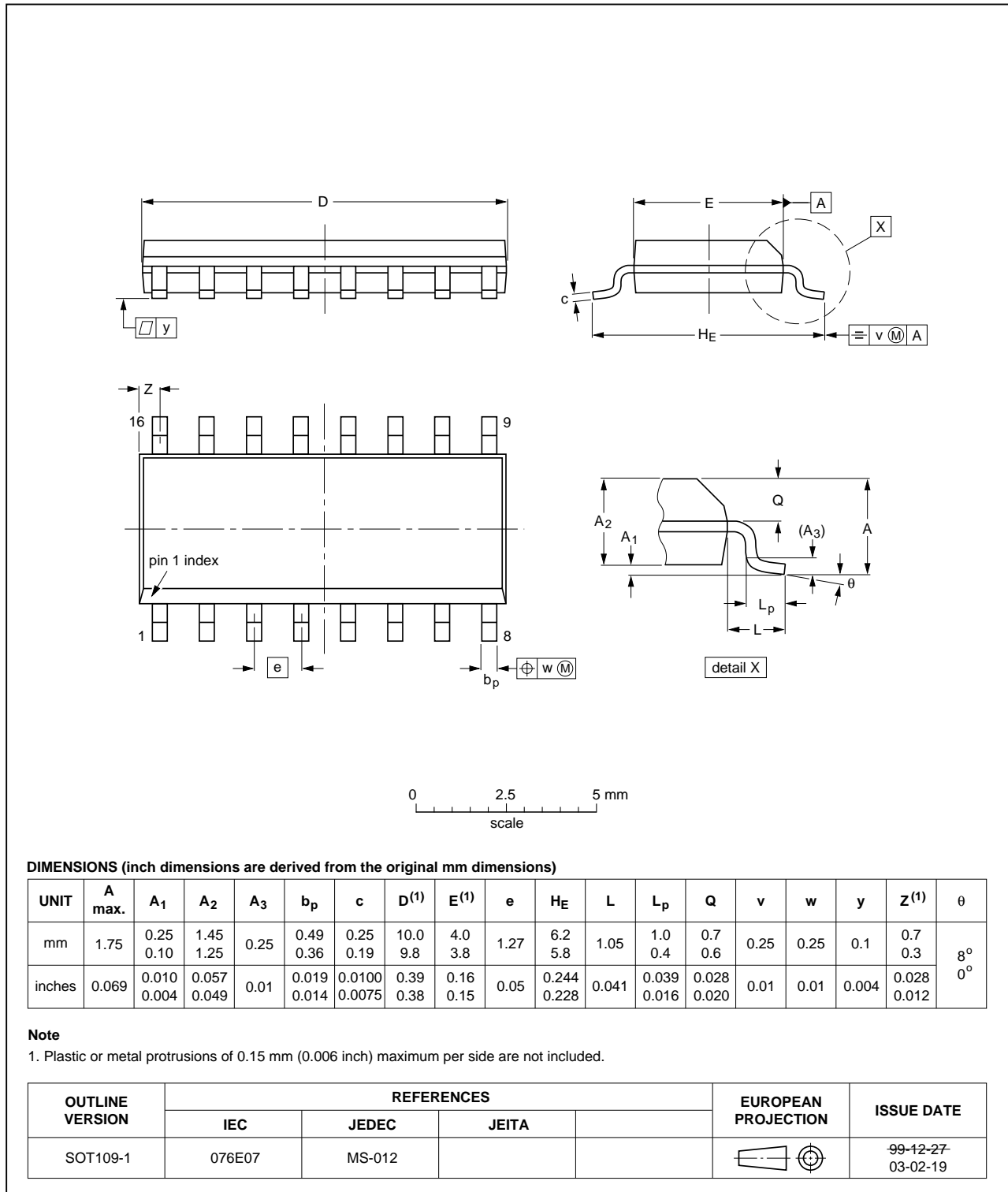


Fig 8. Package outline SOT109-1 (SO16)

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|---|-----------------------|---------------|------------------|
| HEF4044B v.10 | 20111118 | Product data sheet | - | HEF4044B v.9 |
| Modifications: | • Table 6 : I _{OH} minimum values changed to maximum | | | |
| HEF4044B v.9 | 20091215 | Product data sheet | - | HEF4044B v.8 |
| HEF4044B v.8 | 20091127 | Product data sheet | - | HEF4044B v.7 |
| HEF4044B v.7 | 20090721 | Product data sheet | - | HEF4044B v.6 |
| HEF4044B v.6 | 20081111 | Product data sheet | - | HEF4044B v.5 |
| HEF4044B v.5 | 20080812 | Product data sheet | - | HEF4044B v.4 |
| HEF4044B v.4 | 20080717 | Product data sheet | - | HEF4044B_CNV v.3 |
| HEF4044B_CNV v.3 | 19950101 | Product specification | - | HEF4044B_CNV v.2 |
| HEF4044B_CNV v.2 | 19950101 | Product specification | - | - |

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15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
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