CD4032A, CD4038A Types

CMOS Triple Serial Adders

Positive Logic Adder – CD4032A

Negative Logic Adder – CD4038A

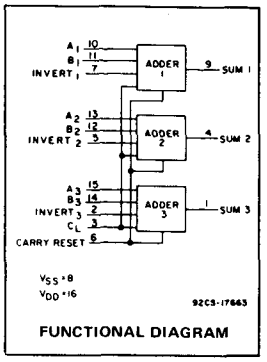
The RCA-CD4032A and CD4038A types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032A or at the negative-going clock for the CD4038A, thus, for spike free operation the input data transitions should occur as soon as possible after the triggering edge.

The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one bit-position before the application of the first bit of the next word. Figs. 2 and 4 show definitive waveforms for all input and output signals.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Invert inputs on all adders for sum complementing applications**
- **Fully static operation. . . . . dc to 5 MHz (typ.)**
- **Buffered outputs**
- **Single-phase clocking**
- **Microwatt quiescent power dissipation. . . . 5 μW (typ.)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**



FUNCTIONAL DIAGRAM

Applications:

- **Serial arithmetic units**
- **Digital correlators**
- **Digital datalink computers**
- **Flight control computers**
- **Digital servo control systems**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATINT GEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . 0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Setup Time, t_S	5 10	t_rCL	–	t_rCL	–	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	2.5 5	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs

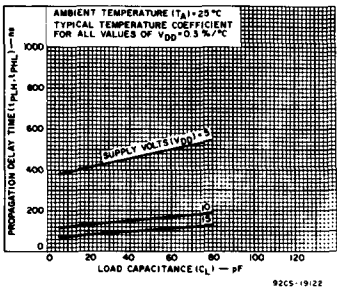


Fig. 1 – Typical propagation delay time vs. load capacitance for A, B, or INVERT inputs to sum outputs.

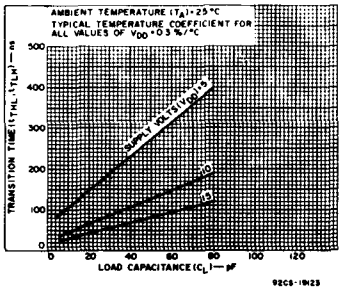


Fig. 2 – Typical transition time vs.load capacitance for sum outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL} A, B, or Invert Inputs to Sum Outputs	5	–	400	1100	–	400	1400	ns
	10	–	125	250	–	125	300	
Clock Input to Sum Outputs	5	–	800	2200	–	800	2400	
	10	–	250	500	–	250	600	
Transition Time; t_{THL}, t_{TLH} (Sum Outputs)	5	–	125	375	–	125	425	ns
	10	–	50	150	–	50	200	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Clock Rise & Fall Time; t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Input Set Up Time, t_S*	5	–	–	t_rCL	–	–	t_rCL	ns
	10							
Average Input Capacitance, C_I		–	5	–	–	5	–	pF

*This characteristic refers to the minimum time required for the A, B, or Reset Inputs to change state following a positive clock transition (CD4032A) or negative transition (CD4038A).

**If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

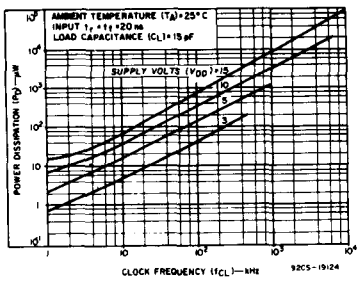


Fig. 3 – Typical dissipation characteristics.

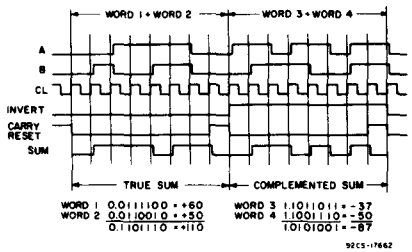


Fig. 4 – CD4032A timing diagram.

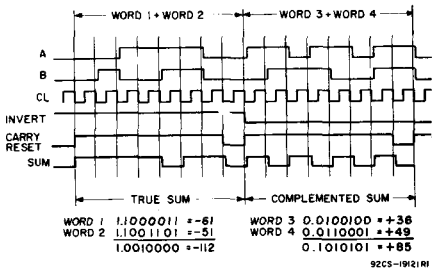


Fig. 5 – CD4038A timing diagram.

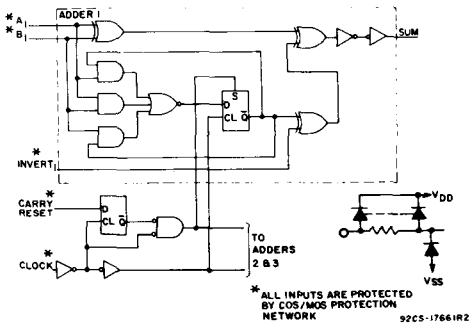


Fig. 6 – CD4032A logic diagram of one of three serial adders.

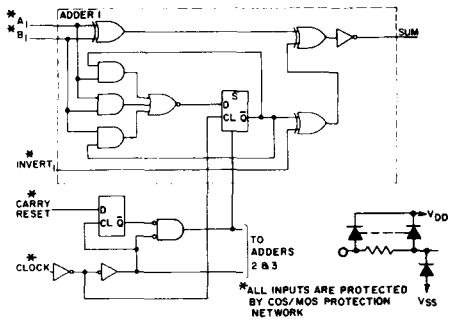


Fig. 7 – CD4038A logic diagram of one of three serial adders.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_DN Min.	0.5	–	5	0.6	0.9	0.5	0.3	0.25	0.9	0.2	0.14	mA
	0.5	–	10	0.75	2.4	0.7	0.6	0.6	2.4	0.5	0.4	
P-Channel (Source), I_DP Min.	4.5	–	5	−0.21	−0.4	−0.15	−0.075	−0.14	−0.4	−0.1	−0.095	
	9.5	–	10	−0.7	−7.2	−0.55	−0.35	−0.3	−1.2	−0.27	−0.22	
Input Leakage Current, I_{IL}, I_{IH}	Any Input			±10⁻⁵ Typ., ±1 Max.								μA
	–	–	15									

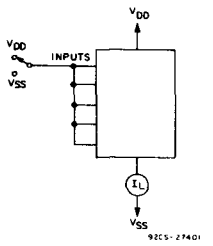


Fig. 8 – Quiescent-device-current test circuit.

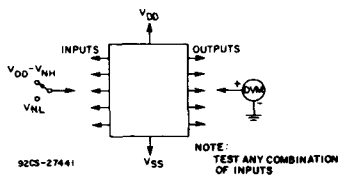


Fig. 9 – Noise-immunity test circuit.

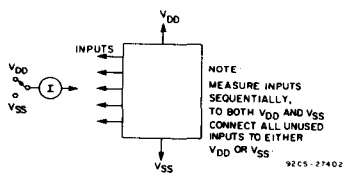


Fig. 10 – Input-leakage-current test circuit.