TBA820 • TBA820L

2-WATT AUDIO AMPLIFIER

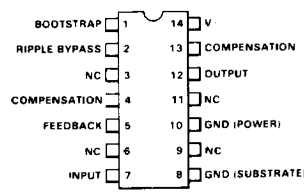
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA820 is an integrated monolithic audio amplifier in a 14-pin plastic power package. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use as a low frequency class B amplifier with wide range of supply voltage (3 to 16 V).

The device is supplied in both the quad in-line (TBA820) and the standard dual in-line (TBA820L).

- **MINIMUM WORKING VOLTAGE OF 3 V**
- **LOW QUIESCENT CURRENT**
- **LOW NUMBER OF EXTERNAL COMPONENTS**
- **GOOD RIPPLE REJECTION**
- **NO CROSS-OVER DISTORTION**
- **TYPICAL OUTPUT POWER:**
  - **–2 W AT 12 V – 8 Ω**
  - **–1.6 W AT 9 V – 4 Ω**
  - **–1.2 W AT 9 V – 8 Ω**
  - **–0.75 W AT 6 V – 4 Ω**

CONNECTION DIAGRAM
14-PIN POWER DIP
(TOP VIEW)
PACKAGE OUTLINE 9A, 9C



ORDER INFORMATION

TYPE	**PART NO.**
820 (9C)	**TBA820**
820L (9A)*	**TBA820L**

*Recommended for new designs.

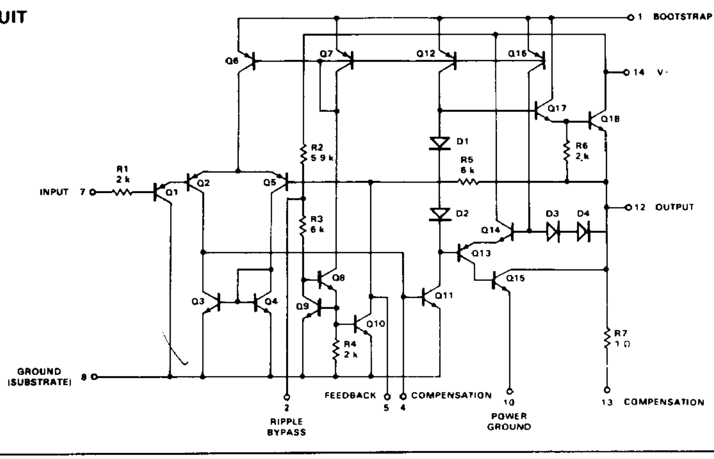
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	16 V
Output Peak Current	1.5 A
Power Dissipation at T_{amb} = 50°C	1.25 W
Storage and Junction Temperature	−40°C to 150°C
Pin Temperature (Soldering 10 s)	260°C

Thermal Data

$\theta_{j\text{-amb}}$	Thermal Resistance Junction-Ambient (copper frame) max	80°C/W

EQUIVALENT CIRCUIT



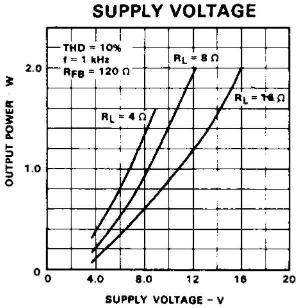
*Planar is a patented Fairchild process

ELECTRICAL CHARACTERISTICS: Power output measured at pin 12, TA = 25°C unless otherwise specified.

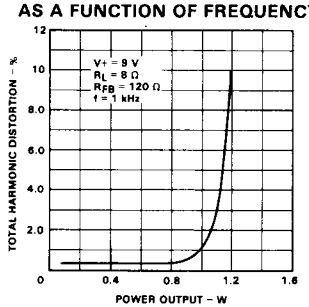
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		3		16	V
Quiescent Output Voltage (Pin 12)	V+ = 9 V	4	4.5	5	V
Quiescent Drain Current	V+ = 9 V		4	12	mA
Bias Current (Pin 7)	V+ = 9 V		0.1	0.7	μA
Power Output, Figure 1	THD = 10%, R_{FB} = 120 Ω, f = 1 kHz, V+ = 12 V, R_L = 8 Ω V+ = 9 V, R_L = 4 Ω V+ = 9 V, R_L = 8 Ω V+ = 6 V, R_L = 4 Ω V+ = 3.5 V, R_L = 4 Ω	 0.9 	 2 1.6 1.2 0.75 0.22		 W W W W W
Input Sensitivity, Figure 1	P_{OUT} = 1.2 W, R_L = 8 Ω, V+ = 9 V, f = 1 kHz R_{FB} = 33 Ω R_{FB} = 120 Ω		 16 60		 mV mV
Input Sensitivity, Figure 1	P_{OUT} = 50 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz R_{FB} = 33 Ω R_{FB} = 120 Ω		 3.5 12		 mV mV
Input Resistance			5		MΩ
Frequency Response (−3 dB) Figure 1	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω C_{FB} = 680 pF C_{FB} = 220 pF		25 – 7000 25 – 20,000		Hz Hz
Total Harmonic Distortion Figure 1	P_{OUT} = 500 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz R_{FB} = 33 Ω R_{FB} = 120 Ω		 0.8 0.4		 % %
Voltage Gain (Open Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz		75		dB
Voltage Gain (Closed Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz R_{FB} = 33 Ω R_{FB} = 120 Ω	 31	 45 34	 37	 dB dB
Input Noise Voltage	V+ = 9 V, BW (−3.0 dB) = 25–20,000 Hz		3		μV
Input Noise Current	V+ = 9 V, BW (−3.0 dB) = 25–20,000 Hz		0.4		nA
Signal Plus Noise to Noise Ratio	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω BW (−3.0 dB) = 25–20,000 Hz R_1 = 100 kΩ, P_{OUT} = 1.2 W		 70		 dB
Supply Voltage Rejection, Figure 2	V = 9 V, R_L = 8 Ω, f (ripple) = 100 Hz, C6 = 50 μF, R_{FB} = 120 Ω		42		dB

TYPICAL PERFORMANCE CURVES

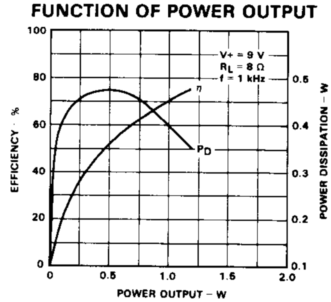
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY

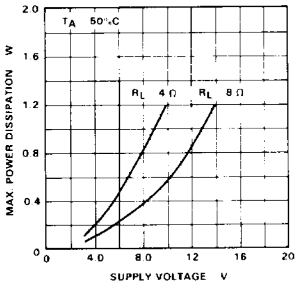


POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT

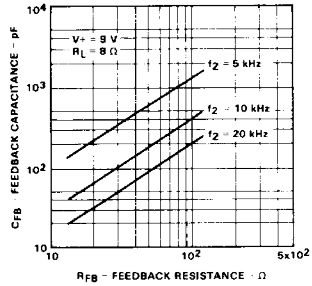


TYPICAL PERFORMANCE CURVES (Cont'd)

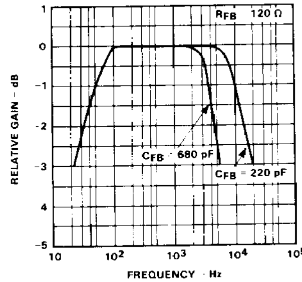
MAXIMUM POWER DISSIPATION (SINE WAVE OPERATION) AS A FUNCTION OF SUPPLY VOLTAGE



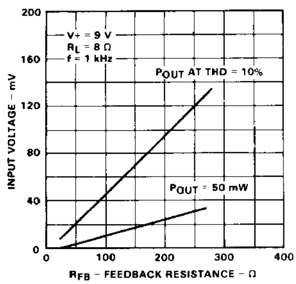
TYPICAL VALUE OF C_{FB} AS A FUNCTION OF R_{FB}



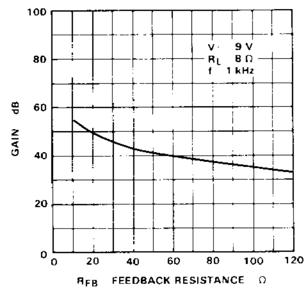
TYPICAL RELATIVE FREQUENCY RESPONSE



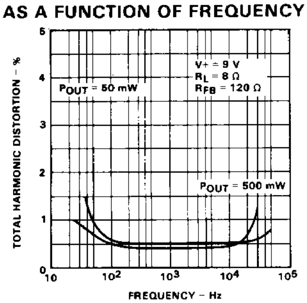
INPUT SENSITIVITY AS A FUNCTION OF R_{FB}



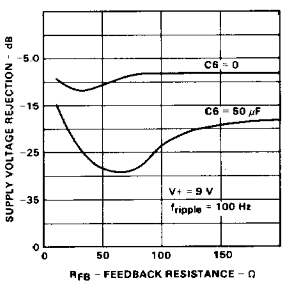
TYPICAL VOLTAGE GAIN (CLOSED LOOP) AS A FUNCTION OF R_{FB}



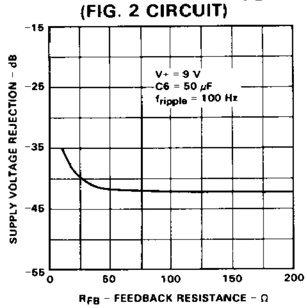
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



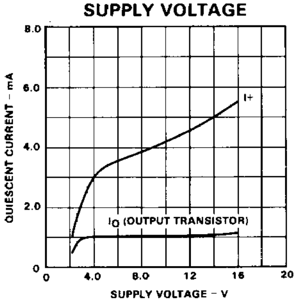
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_{FB} FOR FIG. 1 CIRCUIT



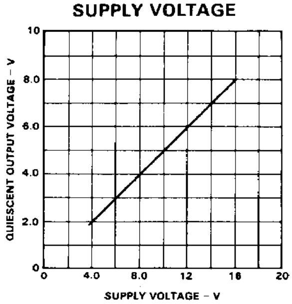
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_{FB} (FIG. 2 CIRCUIT)



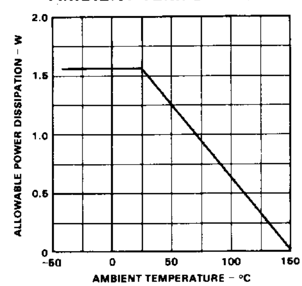
QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



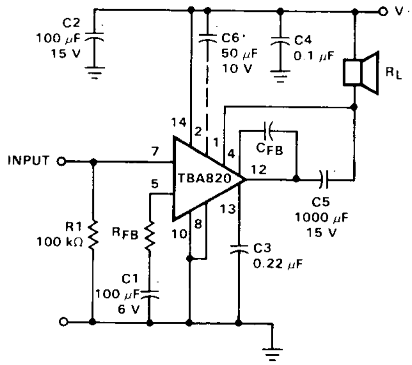
QUIESCENT OUTPUT VOLTAGE AT PIN 12 AS A FUNCTION OF SUPPLY VOLTAGE

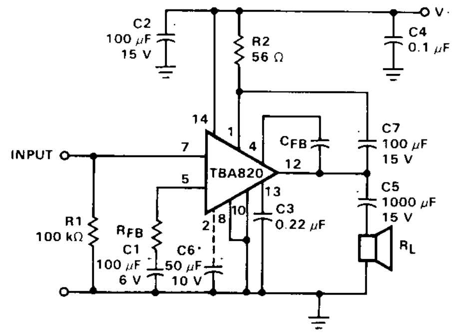


POWER RATING CHART AS A FUNCTION OF AMBIENT TEMPERATURE



TEST AND APPLICATION CIRCUITS





*Capacitor C6 must be used when high ripple rejection is desired.

Fig. 1. Circuit Diagram with Load Connected to the Supply Voltage

Fig. 2 Circuit Diagram with Load Connected to Ground

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